IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Currently Amended): A nonvolatile semiconductor memory comprising:

first cell units each comprising one memory cell and two select gate transistors between which the memory cell is held;

a word line connected in common to each memory cell of the first cell units;

bit lines individually connected to the first cell units;

sense amplifiers disposed for the bit lines; and

an erase circuit which divides the first cell units into blocks and which sets potentials of the bit lines by a block unit at an erase time;

wherein the erase circuit comprises high-voltage transistors which supply an erase potential to the bit lines; and

the high voltage transistors in the same block are controlled by the same column selection signal.

Claim 2 (Original): The nonvolatile semiconductor memory according to claim 1, wherein each of the blocks comprises two or more first cell units.

Claim 3 (Original): The nonvolatile semiconductor memory according to claim 1, wherein each of the blocks includes the first cell units for one byte.

Claim 4 (Original): The nonvolatile semiconductor memory according to claim 1, wherein at the erase time, data is erased by the block unit.

Claim 5 (Original): The nonvolatile semiconductor memory according to claim 1, wherein at a data renewal time, data is erased with respect to at least one block which is a renewal object and data program is executed with respect to at least one block.

Claim 6 (Original): The nonvolatile semiconductor memory according to claim 1, wherein at a data renewal time, the data is erased with respect to all the blocks and data program is executed with respect to all the blocks.

Claim 7 (Canceled).

Claim 8 (Currently Amended): The nonvolatile semiconductor memory according to claim [[7]]1, wherein the high ~~withstand pressure~~ voltage transistor which can bear the erase potential is

connected between the bit lines and sense amplifiers.

Claim 9 (Original): The nonvolatile semiconductor memory according to claim 1, wherein wells are disposed for the blocks, and the first cell units are disposed in the same well by the block unit.

Claim 10 (Original): The nonvolatile semiconductor memory according to claim 1, wherein at the erase time, the data erase comprises: generating a high electric field between

a drain region and control gate electrode of the memory cell which is an erase object; and extracting electrons into the drain region from a floating gate electrode.

Claim 11 (Original): The nonvolatile semiconductor memory according to claim 10, wherein the data is erased by hot hole injection into the floating gate electrode from the drain region.

Claim 12 (Currently Amended): The nonvolatile semiconductor memory according to claim 10, wherein the data is erased by ~~comprises: extracting~~ electrons flowing into the drain region from the floating gate electrode~~; and performing hot hole injection into the floating gate electrode from the drain region~~.

Claim 13 (Original): The nonvolatile semiconductor memory according to claim 1, wherein data write comprises: generating a high electric field between a channel region and control gate electrode of the memory cell which is a write object; and injecting electrons into a floating gate electrode from the channel region.

Claim 14 (Original): The nonvolatile semiconductor memory according to claim 1, wherein each memory cell in the first cell units stores the data of one bit or more.

Claim 15 (Original): The nonvolatile semiconductor memory according to claim 1, further comprising:

second cell units including one or more memory cells; and

one or more word lines connected in common to the second cell units,

wherein the second cell units are individually connected to the bit lines.

Claim 16 (Original): The nonvolatile semiconductor memory according to claim 15, wherein the number of memory cells included in each of the second cell units is equal to that of word lines connected to the second cell units.

Claim 17 (Original): The nonvolatile semiconductor memory according to claim 15, wherein the second cell unit is an NAND cell unit in which memory cells are connected in series.

Claims 18-19 (Canceled).

Claim 20 (Currently Amended): A nonvolatile semiconductor memory comprising:

first cell units each comprising one memory cell and two select gate transistors between which the memory cell is held;

a word line connected in common to each memory cell of the first cell units;

bit lines individually connected to the first cell units;

sense amplifiers disposed for the bit lines; source lines which divide the first cell units into blocks and which are connected to the first cell units;

an erase circuit which sets potentials of the source lines by a block unit at an erase time;

wherein the erase circuit comprises high voltage transistors which supply an erase potential to the source lines; and

the high voltage transistors in the same block are controlled by the same column selection signal.

Claim 21 (Original): The nonvolatile semiconductor memory according to claim 20, wherein each of the blocks comprises two or more first cell units.

Claim 22 (Original): The nonvolatile semiconductor memory according to claim 20, wherein each of the blocks includes the first cell units for one byte.

Claim 23 (Original): The nonvolatile semiconductor memory according to claim 20, wherein at the erase time, data is erased by the block unit.

Claim 24 (Original): The nonvolatile semiconductor memory according to claim 20, wherein at a data renewal time, data is erased with respect to at least one block which is a renewal object and data program is executed with respect to at least one block.

Claim 25 (Original): The nonvolatile semiconductor memory according to claim 20, wherein at a data renewal time, the data is erased with respect to all the blocks and data program is executed with respect to all the blocks.

Claim 26 (Canceled).

Claim 27 (Original): The nonvolatile semiconductor memory according to claim 20, wherein wells are disposed for the blocks, and the first cell units are disposed in the same well by the block unit.

Claim 28 (Original): The nonvolatile semiconductor memory according to claim 20, wherein at the erase time, the data erase comprises: generating a high electric field between a source region and control gate electrode of the memory cell which is an erase object; and extracting electrons into the source region from a floating gate electrode.

Claim 29 (Original): The nonvolatile semiconductor memory according to claim 28, wherein the data is erased by hot hole injection into the floating gate electrode from the source region.

Claim 30 (Currently Amended): The nonvolatile semiconductor memory according to claim 28, wherein the data is erased by ~~comprises: extracting~~ electrons flowing into the drain ~~source~~ region from the floating gate electrode~~; and performing hot hole injection into the floating gate electrode from the source region~~.

Claim 31 (Original): The nonvolatile semiconductor memory according to claim 20, wherein data write comprises: generating a high electric field between a channel region and control gate electrode of the memory cell which is a write object; and injecting electrons into a floating gate electrode from the channel region.

Claim 32 (Original): The nonvolatile semiconductor memory according to claim 20, wherein each memory cell in the first cell units stores the data of one bit or more.

Claim 33 (Original): The nonvolatile semiconductor memory according to claim 20, further comprising:

second cell units including one or more memory cells; and

one or more word lines connected in common to the second cell units,

wherein the second cell units are individually connected to the bit lines.

Claim 34 (Original): The nonvolatile semiconductor memory according to claim 33, wherein the number of memory cells included in each of the second cell units is equal to that of word lines connected to the second cell units.

Claim 35 (Original): The nonvolatile semiconductor memory according to claim 33, wherein the second cell unit is an NAND cell unit in which memory cells are connected in series.

Claims 36-37 (Canceled).

Claim 38 (Currently Amended): A nonvolatile semiconductor memory comprising:

first cell units each comprising memory cells connected in series and two select gate transistors between which the memory cells are held;

second cell units each comprising one memory cell and one select gate transistor;

bit lines which are individually connected to the first cell units and which are individually connected to the second cell units and which are connected in common to the first and second cell units; [[and]]

sense amplifiers disposed for the bit lines, wherein at least an FN tunnel current is used with respect to the respective memory cells in the first and second cell units to perform write/erase; and

an erase circuit which divides the first and second cell units into blocks and which sets potentials of the bit lines by a block unit at an erase time, comprising high-voltage transistors which supply an erase potential to the bit lines,

wherein the high voltage transistors in the same block are controlled by the same column selection signal.

Claim 39 (Cancelled).

Claim 40 (Currently Amended): The nonvolatile semiconductor ~~memory according to claim 38, further~~ comprising:

first cell units each comprising memory cells connected in series and two select gate transistors between which the memory cells are held;

second cell units each comprising one memory cell and one select gate transistor;

bit lines which are individually connected to the first cell units and which are individually connected to the second cell units and which are connected in common to the first and second cell units;

sense amplifiers disposed for the bit lines, wherein at least an FN tunnel current is used with respect to the respective memory cells in the first and second cell units to perform write/erase

source lines which divide the first and second cell units into blocks and which are connected in common to the first and second cell units; and

an erase circuit which sets potentials of the source lines by a block unit at an erase time, comprising high-voltage transistors which supply an erase potential to the source lines;

wherein the high-voltage transistors in the same block are controlled by the same column selection signal.

Claims 41-87 (Canceled).